Evolving Parsimonious Analog Circuits with Sub-circuit Importance and Semantic Awareness

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***Abstract*—Evolutionary circuit design is a challenging task due to the large search space and lack of circuit-interpretability evolutionary operations. Random genetic operations may hinder the identification of useful sub-circuits, leading to stagnation and bloating. In addition, previous circuit evolution lack circuit- semantic information, limiting the algorithm's ability to effectively solve circuit evolution tasks. This work introduces a novel approach for the evolution of analog circuits, leveraging interpretable genetic operations based on Shapley Value Im- portance (SVI) and Circuit-Semantic Similarity (CSS) for tree- based circuit representation. The method efficiently evaluates the importance of sub-circuits, considering device/sub-circuit interdependencies. Moreover, CSS can measure between sub- trees into the evolutionary operations design, preventing the generation of similar sub-circuits with less importance. Our approach outperforms existing methods and human-designed circuits on benchmark and memristive circuits, demonstrating faster convergence and more compact evolved results. Furthermore, its robustness and practical applicability are verified through successful application in evolving memristive FSM-based traffic light system circuits for real-world applications. It achieves circuit tolerance and compactness in different tolerant scenarios.**

***Index Terms*—Evolutionary analog circuit design, tree-based circuit representation, Shapley value, evolvable hardware, genetic programming**